Fast Mixed-Signal System Prototyping using Unique Programmable Analog Array

Jürgen Kampe, Marek Ponca, Uwe Heiber, Andreas Rummler, Christiane Wisser
Technische Universität Ilmenau
Institut für Elektronische Schaltungen und Systeme, 98684 Ilmenau
e-mail : marek.ponca@tu-ilmenau.de

Abstract

Terms like co-design and mixed-signal prototyping have become high attention in the last years, because of the rising need for even shorter time-to-market. Unified solutions for fast design of heterogeneous systems would adequate reduce the overall time needed for their validation as if each subsystem was designed separately. In the following, we will present an unique approach to mixed-signal system evaluation based on the programmable hardware. The problem of the analog subsystem ”on-Chip” prototyping was realized with novel, patented Electrically Programmable Analog Array (EPAA). It was designed for class of sensor signal conditioning problems. EPAA with its fully parameterizable architecture can be configured either at transistor level or using pre-defined function blocks from macro-library. First measurements on a couple of test-cases have proven the suitability of our approach, especially for low-power smart sensors' signal conditioning applications.

1 Introduction

Nowadays rapid prototyping plays a key role in the digital system design. Programmable logic devices based on various principles of configuration storage (GAL, PAL, CPLD, FPGA) overcome the use of ASICs in many application segments, due to their reliability, high performance and ease of use. These features make them suitable for emulation of large systems, whose simulation with either HDL or C based simulators would take an enormous long time.

On the other side, prototyping of analog and mixed-signal systems still takes the main time of the design cycle. New EDA tools, methodologies and models do not exhaustively cover all problems arising by the development of complex VLSI systems. Thus, it is desired to have a solution that would enable the emulation of analog circuits at electrical level prior to their ASIC implementation. There is also need for configurable universal analog solutions with a performance higher than that of solutions built of discrete devices. Success of the programmable logic devices has shown the advantages of reconfigurable hardware. But similar solutions for analog signals are not so easy to find.

In the next, we will propose a new approach to fast prototyping of mixed-signal complex systems based on the use of programmable analog and digital evaluation platforms. Furthermore, we will also describe the architecture and the measurement results of a unique programmable analog chip – Electrically Programmable Analog Array (EPAA). Its architecture and the possible working modes predestine it for the use in signal conditioning. In this case, not the bandwidth or data/sample rate are the bottlenecks of the whole system, but the possibility of adaptive controlling and low power consumption.

2 Rapid System Prototyping

As the need of short time-to-market is stronger as ever before, reliable system verification approach at all levels of abstraction within the whole design flow have to be found. Speedup design cycle, reduction of the redesigns needed and improvement of the prototyping capability are the main requirements of a successful product. Analog and mixed-signal ASIC design usually requires more

than one design cycle, as there is still no reliable physical verification technique available for the analog domain. The reason can be seen in a careless design, neglecting some physical effects and partially also in technology parameter scattering especially for short-channel transistors and deep-submicron technologies. This article concerns the lowest level of mixed-signal system design, hardware physical implementation.

For the verification of such systems either simulation, formal verification methods, emulation of the functionality with discrete devices, or combination of all of them come into account. Due to the huge amount of resources needed and high time costs of a simulation at lower hierarchy levels (transistor, parasitic simulations), production costs rise rapidly. Big compannies use a farm of thousands of workstations for hardware simulations of new Power-PCs. Emulation of the target systems with programmable devices seems to be more acceptable way.

Our evaluation platform targets embedded mixed-signal systems and Systems on a Chip (SoC), also enabling development of Intellectual Properties (IPs), reusable, characterized blocks with physical information (Hard-Macros). It consists of a commercial ARM-based ASIC Integrator Kit and an EPAA daughter-board, so that all features of target mixed-signal system can be easily integrated and emulated. Simplified view can be seen in the Fig. 1.

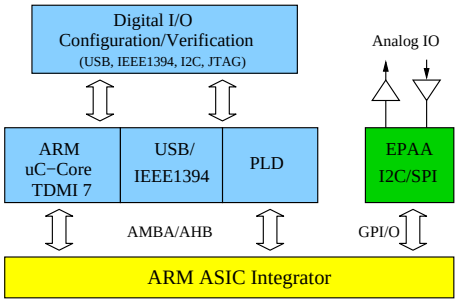

Fig. 1: RDK – Rapid Development Kit for mixed-signal systems

The most critical part in a mixed-signal IC design is the analog part of the chip. For example Infineon's GSM Baseband IC consists of 20% analog and 80% digital components. But the design effort for the analog part was 80%, for the digital only 20% of the design time. It can be seen, how important the disposal of early verification is.

2.1 Analog is the Key

As the analog signal processing is the most significant part of the system verification, there is a need for a simple approach to prototyping and evaluation of analog systems. One way for emulating analog subsystem is to convert analog inputs into their digital counterparts, process them and then convert the results back to analog ones. The main drawbacks of such approach were lower accuracy, for recurrent signal flow maybe unacceptable, and slower maximal data processing rate due to the conversion delays. The way is to implement special purpose programmable devices acting as configurable analog signal processing arrays.

Field programmable analog arrays (FPAAs) meet especially in the last period higher interests as ever before. Pure digital implementations can not supply sufficient efficiency in certain application fields, resulting in the return to analog solutions. As mentioned above, average design-cycle time for analog or mixed-signal design lays above that for digital designs. In order to reduce it and simultaneously make the verification more extensive, we have addressed analog hardware-based emulation, as this proposes more flexible and accurate results as the system simulation.

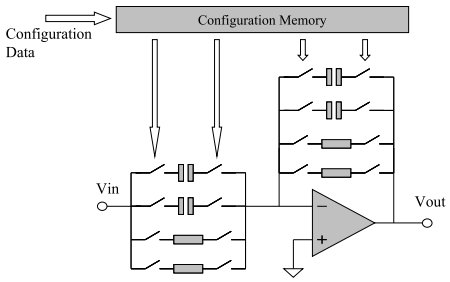

Fig. 2: Principle of programmable analog arrays

Principle of FPAAs is shown in the Fig. 2. Various filter characteristics can be achieved by changing the signal path. Additionally, also sizing of passive/active elements can be programmable.

One specific application of such partial block is shown in the Fig. 3. Adaptive filter seeks in the whole broadband for a tone and detects its appearance.

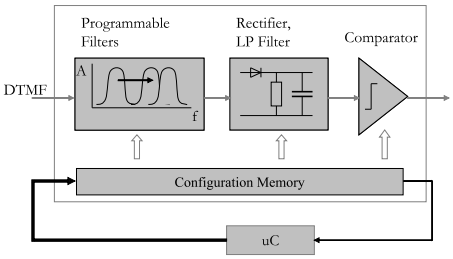

Fig. 3: Dual-tone multi-frequency decoder using adaptive filter implemented in an FPAA

2.2 Programmable Analog Arrays

Programmable analog devices built on a chip, that can be used as IP-cores or as stand-alone analog solutions have became a significant market segment in the last couple of years. The reasons are lower NRE costs opposite to full-custom analog ASICs, lower design effort due to the supporting development software and shorter design time (no re-spins needed). Field programmable arrays, either gate arrays or analog arrays, provide numerous advantages over discrete design including high integration density and reliability, fast turn-around design cycle, lower mass, volume and power consumption. Traditionally, standard mixed-signal circuits were used for industrial applications almost always implemented with discrete devices, because the costs were opposite to ASIC implementation still too big.

Specific FPAAs containing also AD/DA converters for mixed-signal processing are sometimes referred to as Field Programmable Mixed-signal Arrays (FPMA). Incorporated logic parts are relative small, placed close to analog ones, allowing for simple digital processing without need for external FPGA. For the purpose of prototyping and rapid development, short-time reconfigurability must be supplied. Therefore only FPAAs with their own development software and direct download options can be used for fast emulation. Summary of currently commercially available FPAAs (Anadigm, Zetex, Cypress, Lattice) can be found in [1]. Each vendor supplies also appropriate design software for its FPAAs. However, none of them offers a ”full-custom” programming capability, users can only connect predesigned, partial parameterizable analog macroblocks, but they cannot build their own functional blocks.

There are also several other university research groups concentrating on the design of programmable analog arrays. Edwards from John Hopkins University (Maryland) has proposed in [2] an one-time programmable FPAA based on Actel’s Metal-to-Metal antifuse technology, desired for space-flight applications. Premont (University of Lyon) presented in [3] an FPAA utilizing current conveyors connected to a common current rails, where the switch resistance has only little effect on current-mode circuits. Continuous-time, as in [4] and switched-capacitor approaches [5] have became their attention. Becker and Manoli have proposed a continuous-time FPAA based on reconfigurable G_M cells [6].

Special-purpose programmable devices are needed, if the whole functionality of a mixed-signal system should be faithfully implemented and emulated. For emulation of analog subsystems, we propose Electrically Programmable Analog Array – EPAA. This device suffers from the drawbacks of its counterparts produced commercially and exploits basic principles of programmable devices. Granularity was refined from block to transistor level. In-field parameter adjustment and topology configuration designates the EPAA to be used in sensor and actuator technology, or signal conditioning. Additional to [7], we will introduce our EPAA as it could be included in a system for rapid mixed-signal prototyping. We will also present first measurement results of the prototype.

3 Electrically Programmable Analog Array – EPAA

Compared to commercially available FPAAs, our EPAA serves more degrees of freedom, due to its fine granularity, supposing its use not only as sensor signal conditioning unit, but also as prototyping device for mixed-signal ASIC designers, or training chip for ASIC-design education classes.

3.1 Architecture

EPAA is a fully configurable analog array dedicated for implementation of analog and mixed-signal applications using both, continuous current (CC) and switched-capacitor (SC) techniques (e.g. sensor/actuator technology, com-

munication, signal conditioning, controlling etc.). Overall architecture overview can be seen in Fig. 4. Partitioning to 4 clusters (each containing 4 cells) can be seen in the right-upper part. Clock scheme generators enabling SC techniques are on the left side. Mixed-signal capability serve four cascadable AD/DA converters working in various modes, associated in pairs to cluster-columns, together with digital data/control high/low speed buses. Desired EPAA configuration is autonomous downloaded via serial system interface from EEPROM, immediately after power-on sequence, activating appropriate connections between elementary devices inside the EPAA analog core.

These build together signal paths (switch-matrices), or bigger devices (device-size rating switches). Also proper AD/DA conversion and SC-clock generation scenarios are set in the digital configuration registers. Simple configuration scheme (either serial shift through the analog core), or parallel write to digital registers allows for in-field parameter adjustment and topology modification (desired in sensor-signal interfaces and processing devices) by external microcontroller.

Product	Applications	Macro Blocks
Anadigm (Anadigm)	analog filters, data acquisition, Audio, RFID ... medical ...	filtering, summation, amplification
ispPAC (Lattice)	analog filters, power sequencing, voltage monitoring, signal conditioning	filtering, summation, amplification, integration
TRAC (Zetex)	multipliers, rectifiers, modulators	addition, log, antilog, negation

Table 1: Commercially available FPAAs

The EPAA layout structure is based on a hierarchical, regular arrangement of devices and reflects common requirements for analog circuit designs. As generally known, the basic components of analog CMOS circuitry are differential amplifiers, current mirrors and transfer gates. Consequently, each of the analog array's cells contains all devices necessary for building these components: differential transistor pair, load transistor pair and current mirror transistor pair. Depending on the type of differential transistor pairs, we distinguish between two basic cell types: N-Cells (in Fig. 5) and adequate P-Cell. In

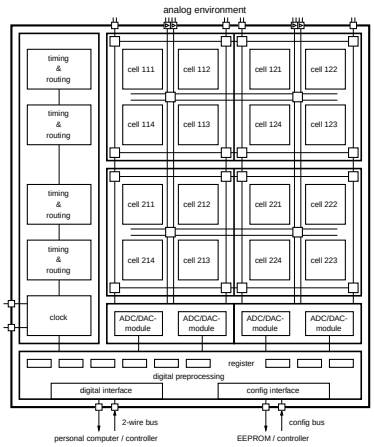

Fig. 4: EPAA - Architecture. Two buses (high- und low- speed) for configuration and data exchange

addition to the load transistors, all cells contain also sizeable passive devices: resistors with high resistance values in combination with poly-Si capacitors as well as feedback resistors especially intended for series feedback. The channel conductance type of the differential pair determines the cells to be called N- or P-cell. A cluster is formed by two N- and two P-cells arranged in a chequered pattern. This way, the regular structure leads to a predictable device coupling. The set of devices in each cluster can be used to implement a wide variety of functional blocks such as phase-shifter, multiplier, amplifier, VCO, filters etc. There is an analog-macro library available, containing parameterizable functional blocks optimized for the EPAA architecture. Possible ap-

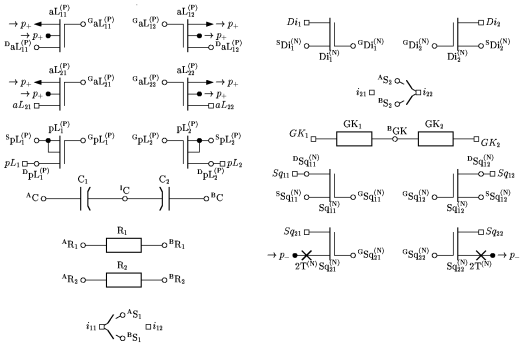

Fig. 5: EPAA: N-Cell Primitives

plication areas can be seen not only in analog subsystem prototyping, but also for instance in signal processing (amplification, summation, filtering, integration etc.), sensor signal condition-

ing, analog front-end for data acquisition, precision voltage monitoring, automated test and measurements, power supply sequencing, differential signaling etc.
Initial version of EPAA was implemented in Alcatel Mietec 0.5 μm CMOS technology, comprising 2×2 programmable clusters. Part of the digital configuration and communication circuitry is implemented in an additional FPGA, allowing direct access to AD/DA modules. Therefore PGA120 package had to be used, contrary to the initial idea of a small programmable analog array with mixed-signal capabilities. Final version of the EPAA chip will be implemented completely in a CLCC44 (DIL28) package, communicating with the digital subsystem via two 2-wire buses.
The main EPAA features can be summarized as follows:

- Architecture: 2x2 Clusters, 4 cells per Cluster (2xPcell, 2xNcell)
- 22 scalable elements in each cell (12xMOS, 4xR, 2xC, 4xclocked switches)
- 12 analog pins, 8 analog pins with additional driver circuit
- 4 AD/DA modules, various conversion-schemes possible (SAR, integrating, flash, pipelined, $\Sigma\Delta$ etc.)
- Internal autonomous and/or data-depending clock generation, 8 possible duty-cycle variations
- Both CC and SC techniques supported
- Bandwidth of 4 up to 12 MHz (depending on analog pin driver configuration)
- Global configuration time $\approx$ 8ms; Reconfiguration time $\approx 60\mu$s (e.g. AD/DA Mode)
- Low-speed configuration bus, high-speed data bus
- Easily extendable due to the regular structure, and parametric digital design
- Library of functional blocks optimized for effective use of resources

Advanced ASIC designers will profit from the possibility of manual transistor-level schematic-based design, placement and routing, as they will be able to create their own reusable functional blocks optimized for the desired analog subsystem. Intermediate users can prototype and evaluate their block-based designs without deep knowledge about EPAA structure, profiting from design block library. EPAA can be also used as IP core, for later mixed-signal SoC applications.

3.2 Results

RDK research project comprises two tape-outs, both in mixed-signal CMOS 0.5μm technology. First prototype, with die size of 6.3×5.5 mm, assembled in PGA 120 package, is already being measured. Part of the digital configuration and communication circuitry is implemented in an additional FPGA, allowing direct access to AD/DA modules. For detailed overview, see Table 2.

Parameter	**Simulation**	**Maesurement**
V_{DD}	3.3 V $\pm$ 10%	3.3 V $\pm$ 10%
I_{DD}	10 mA	15 mA
I_{DD} (low power)	$\leq 1\,\mu$A	$\leq 10\,\mu$A
Impedance-converter : IN Mode		
Bandwidth	4.1 MHz	6.6 MHz
Offset	7.5 mV	5.1mV
A_u	0.98	0.96
Impedance-converter : OUT Mode		
Bandwidth	12.4 MHz	22 MHz
Offset	3.5 mV	69.1 mV
A_u	0.997	0.98
Impedance-converter : INOUT Mode		
Bandbwidth	4.0 MHz	5.1 MHz
Offset	54.1 mV	67.8 mV
A_u	0.994	0.99
Diff. Amplifier in Analog Core ($C_L = 2$ pF)		
Bandwidth	7.6 MHz	7.1 MHz
Offset	0.1 mV	1.5 mV
A_u	40 dB	31 dB
VCO in Analog Core		
f_{MIN}	322 kHz	312 kHz
f_{MAX}	4.5 MHz	3.8 MHz
V_{OUT} (f_{MIN})	331 mV	340 mV
V_{OUT} (f_{MAX})	321 mV	322 mV

Table 2: Results of the first realization. $V_{DC} = 1.65$ V*;* $R_L = 16.5\,k\Omega$*;* $C_L = 32$ pF

4 EPAA Design Software

Dedicated design tools have to be used for special purpose electronic devices, as they are unique in their architecture and paradigm. We have developed Java-based Eclipse plug-in "Corona", meant to support the whole design flow from initial idea, up to the final configuration stream generation and download to EPAA, without the need of any commercial EDA tool.
Corona works on various abstraction levels, it can be used for macro-block or transistor-level

placement, (manually or automatically). Routing is also supported either in manual or automatic mode (final user modifications are allowed). For the simulation of the designed circuits, it is intended to embed Berkeley SPICE into Corona. There are three possible design views, depending on the user expertise level and the abstraction needed for specific design. "Author view" suffers of all abstraction, regarding the functionality of the created circuit. It is used for debugging and characterization in prototyping phase of the EPAA project. Ragular users, even expert ones, do not need the exhausting information about array connections in such a detailed matter. "Expert view" allows analog and mixed-signal circuit design, as IC-designer do, at transistor level, with 3 degrees of freedom : pasive devices sizing, active devices sizing and connecting. "Application view" allows for system design at functional-block level, utilising libraries of pre-designed macro blocks.

5 Conclusion

Our goal is to meet the needs for short mixed-signal systems' prototyping time and low-cost development of analog circuits especially for sensor/actuator technology. Using the RDK evaluation platform, emulation of complex mixed-signal systems can be done within short design cycle. Proposed programmable analog array EPAA can be used as a fully configurable mixed-signal SoC or as a hardware IP for the use in more complex systems. Its in-field parameter adjustment and topology modification features, together with ease of use qualify it for the use in many application areas described above.

References

[1] E. Mackensen, D. Arnold, and W. Kuntz, "Fpaas und psocs für die analoge signalaufbereitung von sensor-/aktordaten in intelligenten, autarken mikrosystemen (iam)," in *Analog2003*, Heilbronn, Germany, September 10-12 2003, VDE, pp. 185–190.

[2] R.T. Edwards, K. Strohbehn, S.E. Jaskulek, and R. Katz, "Analog module architecture for space-qualified field-programmable mixed-signal arrays," in *2nd annual Military and Aerospace Applications of Programmable Devices and Technologies Conference (MAPLD)*, Laurel, Maryland, USA, October 1999.

[3] C. Premont, R. Grisel, N. Abouchi, and J. Chante, "A current conveyor based field programmable analog array," *Analog Integrated Circuits and Signal Processing*, vol. 17, no. 1-2, pp. 105–124, September 1998.

[4] B. Pankiewicz, M. Wojcikowski, S. Szczepanski, and Y. Sun, "A field programmable analog array for cmos continuous-time ota-c filter applications," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 125–136, February 2002.

[5] Lee E.K.F. and Hui W.L., "A novel switched-capacitor based field-programmable analog array architecture," *Kluwer Analog Integrated Circuits and Signal Processing – Special Issue on Field Programmable Analog Arrays*, vol. 17, no. 1-2, pp. 35–50, September 1998.

[6] J. Becker and Y. Manoli, "A Continuous-Time Field Programmable Analog Array (fpaa) Consisting of Digitally Reconfigurable g_M-Cells," in *Proceedings of the 2004 International Symposium on Circuits and Systems - ISCAS '04*, Vancouver, Canada, May 23-26 2004, IEEE, vol. 1, pp. 1092–1095.

[7] J. Kampe, G. Scarbata, S. Arlt, M. Ponca, A. Rummler, U. Heiber, and Ch. Wisser, "Rdk–Rapid Develepment Kit for Mixed-Signal Systems," in *27th International Spring Seminar on Electronics Technology – ISSE2004*, Sofia, Bulgaria, May 13-16 2004, IEEE.