RDK – Rapid Development Kit for Mixed-Signal Systems

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Abstract

The goal of evaluation platforms is design time and verification costs reduction, as these are the main parameters affecting time to market and final success of a product. Following article describes a new approach to prototyping of complex mixed-signal systems, suitable especially as a platform for system developers. Both, digital and analog subsystems can be emulated within one development kit. Digital part is based on the ARM ASIC-Integrator Kit, targeting rapid development of embedded applications. Patented Electrically Programmable Analog Array (EPAA) acts as the part morphing the functionality of the analog subsystem. EPAA with fully parametrizable architecture allows either for transistor-level design of various analog function blocks, or reuse of pre-designed macros. In-field parameter adjustment and topology configuration designates the EPAA to be used in sensor and actor technology, or signal conditioning. Dedicated configuration software has been developed, allowing for various modi of device configuration, depending on the designer's experience and used abstraction level. *Keywords:* mixed-signal, FPAA, SoC, ASIC

Introduction

As the need of short time-to-market is stronger as never before, there is a need of reliable system verification at all levels of abstraction within the whole design flow. Speedup design cycle, reduction of the redesigns needed and improvement of the prototyping capability are the main requirements of a successful product. Analog and mixed-signal ASIC design usually requires more than one design cycle, as there is still no reliable physical verification technique available for the analog domain. The reason can be seen in a careless design, neglecting some physical effects, and partially also in technology parameter scattering especially for short-channel transistors and deep-submicron technologies. This article concerns the lowest level of mixed-signal system design, its physical implementation.

For the verification of such systems either simulation, formal verification methods, emulation of the functionality, or combination of all of them comes into account. Due to the huge amount of resources needed and high time costs of a simulation at lower hierarchy levels (transistor, parasitic simulations), production costs rise rapidly. Emulation of the target systems with programmable devices seems to be more acceptable way.

In the next, a sophisticated way for prototyping and verification of mixed-signal systems will be presented, where the main attention will be given on the analog programmable solution. To fulfil the fast analog prototyping requirements, we have developed and implemented a novel-architecture analog programmable array, as described in the second part.

Rapid Development Kit

Rapid prototyping plays nowadays a key role in the digital system design. Programmable logic devices based on various principles of configuration storage (GAL, PAL, CPLD, FPGA) overcome the use of ASICs in many application segments, due to their reliability, high performance and ease of use. These features make them suitable for emulation of large systems, whose simulation either with HDL, or C based simulators would take enormous long time.

Processor emulation allows for speedup in order of 10-10^3 opposite to commercial HDL cycle based simulator, or simulation in C. For instance Tensilica extension kit executes up to 33 millions of processor cycles, typical HDL-simulator executes 2 up to 10 thousands of cycles.

The Amo's Venus-X rapid prototyping platform enables accelerated ASIC design verification as well as hardware assisted software debugging and implementation at a remarkably early stage of product development process. The system mainly consists of two core units, each carrying up to three Xilinx Virtex-II FPGAs with more than 1,000 I/O signals.

Other approach is the use hundreds of workstations building a computer cluster, used as a huge hardware simulator, as the IBM TJ Watson Research Centre does by design of new PowerPCs. The cluster works as a distributed-mode processor simulation environment, with the high amount of used cluster nodes, what makes its operating expenses enormous and inapplicable.

Our evaluation platform targets embedded mixed-signal systems and Systems on a Chip (SoC), also enabling development of Intellectual Properties (IPs), reusable, characterised blocks with physical information (Hard-Macros). It consists of a commercial ARM-based ASIC Integrator Kit and an EPAA daughterboard, so that all features of target mixed-signal system can be easily integrated and emulated. Simplified view can be seen of the Fig. 1.

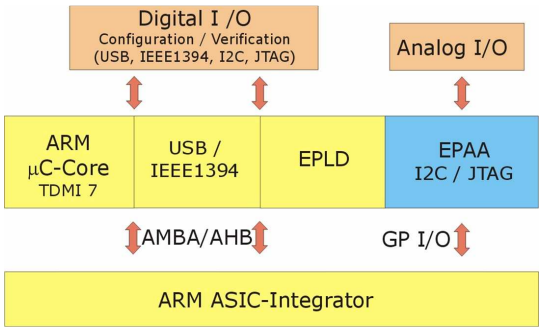

Fig. 1. Rapid Development Evaluation Platform

Analog is the Key

As the analog signal processing is the most significant part of the system verification, there is a need for a simple approach to prototyping and evaluation of analog systems. One way for emulating analog subsystem is to convert analog inputs into their digital counterparts, process them and then convert the results back to analog ones. The main drawbacks of such approach were lower accuracy, for recurrent signal flow maybe unacceptable, and slower maximal data processing rate due to the conversion delays. The way is to implement special purpose programmable devices acting as configurable analog signal processing arrays.

Field programmable analog arrays (FPAAs) meet especially in the last period higher interests as ever before. Pure digital implementations can not supply sufficient efficiency in certain application fields, resulting in the return to analog solutions. As mentioned above, average design-cycle time for analog or mixed-signal design lays above that for digital designs. In order to reduce it and simultaneously make the verification more extensive, we have addressed analog hardware-based emulation, as this proposes more flexible and accurate results as the system simulation.

Special-purpose programmable devices are needed, if the whole functionality of a mixed-signal system should be faithfully implemented and emulated. For emulation of analog subsystems, we propose Electrically Programmable Analog Array (EPAA).

This device suffers from the drawbacks of its counterparts produced commercially and exploits basic principles of programmable devices. Granularity was refined from block to transistor level. Currently commercially available FPAAs can be seen in the Table 1. Each vendor supplies also appropriate design software for its FPAAs. Actually none of them offers a “full-custom” programming capability, users can only connect predesigned, partial parametrizable analog macro-blocks, but they cannot build them their own functional blocks.

There are also several other university-based FPAA research groups (Lyon, Edinburgh, Nottingham, Illinois, Portland, Alberta, Maryland). One of them (Lyon) is working on a FPAA utilizing current conveyors connected to a common current rails, where the switch resistance has only little effect on current-mode circuits. Other (Nottingham) is working on a switched-current design. John Hopkins University (Maryland) has proposed one-time programmable FPAA based on Actel’s Metal-to-Metal antifuse technology, desired for spaceflight applications. Main FPAA challenges that have to be considered and the ways for their handling can be seen in the Table 2.

Electrically Programmable Analog Array

EPAA is a fully configurable analog array dedicated to implementation of analog and mixed-signal applications using both, continuous current (CC) and switched-capacitor (SC) techniques (e.g. sensor/actor technology, communication, signal conditioning, controlling etc.). Overall architecture overview can be seen on Fig. 2. Partitioning to 4 clusters (each containing 4 cells) can be seen in the right-upper part. Clock scheme generators enabling SC techniques are on the left side. Mixed-signal capability serve four cascadable AD/DA converters working in various modi, associated in pairs to cluster-columns, together with digital data/control high/low speed buses. Desired EPAA configuration is autonomous downloaded via serial system interface from EEPROM, immediately after power-on

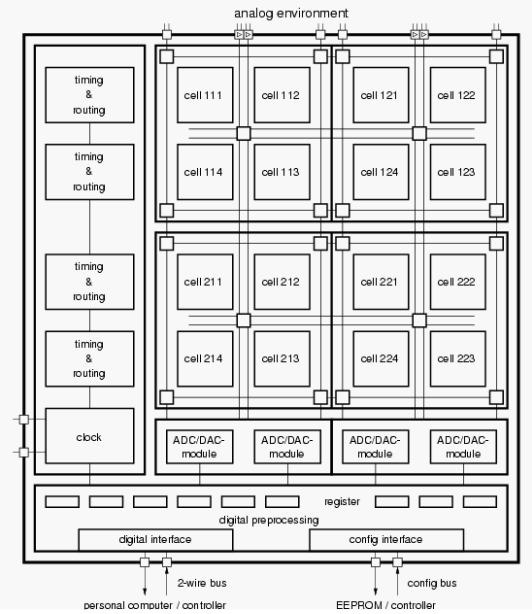

Fig. 2. EPAA – Architectural overview

sequence, activating appropriate connections between elementary devices inside the EPAA analog core.

These build together signal paths (switch-matrices), or bigger devices (device-size rating switches). Also proper AD/DA conversion and SC-clock generation scenarios are set in the digital configuration registers. Simple configuration scheme (either serial shift through the analog core), or parallel write to digital registers allows for in-field parameter adjustment and topology modification (desired in sensor-signal interfaces and processing devices) by external microcontroller.

Table 1. Commercially available programmable Analog Arrays

Product	Target Applications	Macro Blocks
Anadigm -Anadigm	Analog filters, data acquisition, Audio, RFID, Medical …	filtering, summation, amplification
ispPAC -Lattice	Analog filters, power supply sequencing, voltage monitoring, sensor signal conditioning, automated test and measurements …	filtering, amplification, summation, filtering, integration
TRAC -Zetex	Multipliers, rectifiers, modulators	addition, negation, log, antilog, amplification

EPAA layout structure is based on a hierarchical, regular arrangement of devices and reflects common requirements for analog circuit designs. As generally known, the basic components of analog CMOS circuitry are differential amplifiers, current mirrors and transfer gates. Consequently, each of the analog array's cells contains all devices necessary for building these components: a differential transistor pair, a load transistor pair and a current mirror transistor pair (Fig. 3.). Depending on the type of load transistors, we distinguish between two basic cell types: (1) “Passive” cells apply load transistor pairs of long channel length and (2) “active” cells use current mirror transistor pairs serving as load transistors.

Table 2. Main common challenges in the design of Analog Arrays

Feature	Affected by	Arrangements
Speed	Number of inter-connections	Proper, balanced routing, minimal signal paths
Accuracy	Device matching	Same location, orientation, surrounding environment
Digital Noise	Clock feedthrough	Minimize parallel clock-data feeding, maximize ground planes
Analog Noise	power supply, thermal-, shot-, 1/f noise	Proper analog design
Power Consumption	Stand-by currents, switching activities	Use low-power techniques
Resource Allocation	Quantity and granularity of analog blocks	Allow higher connectivity for special purpose blocks, allow generic blocks for through-routing
Resource Utilization	Resource allocation	Properly allocated blocks, optimized routing

In addition to the load transistors, all cells contain passive devices: straight resistors with high resistance values in combination with poly-Si capacitors as well as feedback resistors esp. intended for series feedback. The channel conductance type of the differential pair determines the cells to be called N- or P-cell. A cluster is formed by two N- and two P-cells arranged in a chequered pattern. This way, the regular structure leads to a predictable device coupling.

The set of devices in each cluster can be used to implement a wide variety of functional blocks such as phase-shifter, multiplier, amplifier, VCO, filters etc. There is an analog-macro library available, containing parametrizable functional blocks optimized for the EPAA architecture.

Possible application areas can be seen for instance in signal processing (amplification, summation, filtering, integration etc.), sensor signal conditioning, analog front-end for data acquisition, precision voltage monitoring, automated test and measurements, power supply sequencing, differential signalling.

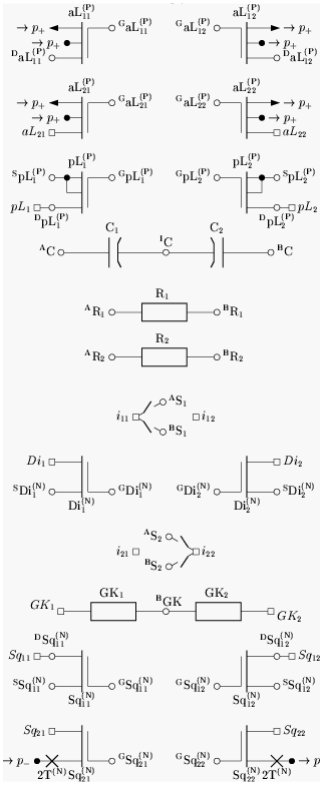

Fig. 3. EPAA N-cell elements

Initial version of EPAA was implemented in Alcatel Mietec 0.5um CMOS technology, comprising 2x2 programmable clusters. Part of the digital configuration and communication circuitry is implemented in an additional FPGA, allowing direct access to AD/DA modules. Therefore PGA120 package had to be used, contrary to the initial idea of a small programmable analog array with mixed-signal capabilities. Final version of the EPAA chip will be implemented completely in a CLCC44 (DIL28) package, communicating with the digital subsystem via two 2-wire buses.

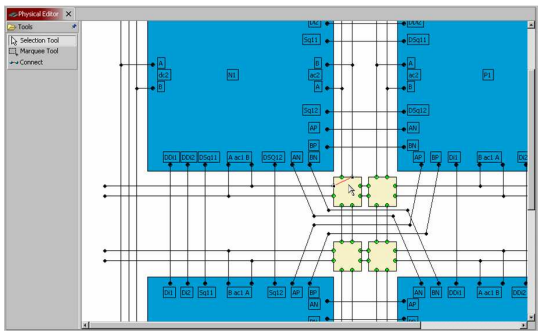

Fig. 4. Corona – screenshot of physical editor, enabling manual signal path routing

EPAA characteristics:

- 2x2=4 Clusters,
- 4 cells in one Cluster (2xPcell, 2xNcell)
- 22 Elements in one cell
- 3x4 dc analog pins (without driver)
- 2x4 ac analog pins (with driver)
- 4 AD/DA modules, various conversion-schemes possible (SAR, dual slope, flash, pipeline)
- Internal autonomous and/or data-depending clock generation
- Both CC and SC techniques supported, 8 possible duty-cycle variations
- Direct connection of various sensitive elements
- Differential signalling possible
- Power supply Vdd= 3.3V, Idmax=10mA
- Low-speed configuration bus
- High-speed data bus
- Easily extendable due to the regular structure, and parametrical digital design

EPAA Configuration Development Tool

Dedicated design tools have to be used for special purpose electronic devices, as they are unique in their architecture and paradigm. We have developed Java-based Eclipse plug-in “Corona”, meant to support whole design flow from initial idea, up to the final configuration stream generation and download to EPAA, without the need of any commercial EDA tool.

Corona works on various abstraction levels, it can be used for macro-block or transistor-level placement, (manually, or automatically). Routing is also supported either in manual or automatic mode (final user modifications are allowed).

Advanced ASIC designers will profit by the possibility of manual transistor-level schematic-based design, placement and routing, as they would be able to create their own reusable functional blocks optimised for the desired system. Intermediate users can prototype and evaluate their block-based designs without deep knowledge about EPAA structure.

Conclusion

Our goal is to meet the needs for short mixed-signal systems’ prototyping time and low-cost development of analog circuits especially for sensor/actor technology. Using the RDK evaluation platform, emulation of complex mixed-signal systems can be done within short design cycle. Proposed programmable analog array EPAA can be used as a fully configurable mixed-signal SoC, or as a hardware IP for the use in more complex systems. Its in-field

parameter adjustment and topology modification features, together with ease of use qualify it for the use in many application areas described above.

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